What Is Claimed Is:

1. A method for processing signals on a programmable logic device that includes a plurality of programmable logic regions, the method comprising:

configuring at least one of the regions as word conditioning logic;

configuring at least another one of the regions as a computation unit having an input, an output, and a critical path, wherein the computation unit is configured to propagate signals from the input to the output via the critical path without propagating the signals through the word conditioning logic; and

providing a datapath from the output of the computation unit to a storage destination, wherein signals on the datapath are propagated through the word conditioning logic.

2. The method defined in claim 1, further comprising:

providing rounding logic in the word conditioning logic.

3. The method defined in claim 1, further comprising:

providing saturation logic in the word conditioning logic.

4. The method defined in claim 1, further comprising:

providing rounding logic and saturation logic in the word conditioning logic, wherein the rounding logic and the saturation logic are arranged in series.

5. The method defined in claim 4, further comprising:

monitoring the signals in the computation unit using the saturation logic.

6. The method defined in claim 5, wherein the monitoring is performed by monitoring circuitry included in the saturation logic, wherein the monitoring circuitry is operated separately from and in parallel with the computation unit.

7. The method defined in claim 1, further comprising:

configuring at least a further one of the regions as analysis logic.

8. The method defined in claim 7, further comprising:

performing an analysis operation in the analysis logic in combination with a write operation to the storage destination.

9. The method defined in claim 7, further comprising:

performing an analysis operation in the analysis logic in combination with a move operation to the storage destination.

10. The method defined in claim 7, wherein the analysis logic is configured to perform block floating point analysis.

11. A programmable logic device, comprising:

a computation unit having an input, an output, and a critical path, wherein the computation unit is configured to propagate signals received on the input to the output via the critical path without propagating the signals through word conditioning logic; and

a datapath configured to convey output signals from the computation unit to a storage destination, wherein the output signals on the datapath are propagated through word conditioning logic.

12. The device defined in claim 11, wherein the computation unit includes an arithmetic logic unit in the critical path, wherein the arithmetic logic unit does not include word conditioning logic.

13. The device defined in claim 11, wherein the computation unit includes an accumulator in the critical path, wherein the accumulator does not include word conditioning logic.

14. The device defined in claim 11, further comprising:

a first logic substructure containing word conditioning logic and having an associated input and an associated output, wherein the associated input of the first logic substructure is coupled to the output of the computation unit and the associated output of the first logic substructure is coupled to the datapath.

15. The device defined in claim 14, wherein the word conditioning logic contained in the first logic substructure is configured to perform rounding and saturation operations.

16. The device defined in claim 11, further comprising:

a plurality of memory circuits, wherein the storage destination is at least one of the plurality of memory circuits.

17. The device defined in claim 11, further comprising:

a plurality of registers, wherein the storage destination is at least one of the plurality of registers.

18. The device defined in claim 11, further comprising:

a second logic substructure containing analysis logic and having an associated input and an associated output, wherein the associated input of the second logic substructure is coupled to the datapath.

19. The device defined in claim 18, wherein the analysis logic contained in the second logic substructure is configured to perform block floating point analysis.

20. The device defined in claim 18, wherein the analysis logic contained in the second logic substructure is executable in combination with a write operation to the storage destination.

21. The device defined in claim 18, wherein the analysis logic contained in the second logic substructure is executable in combination with a move operation to the storage destination.

22. A digital processing system, comprising:

processing circuitry;

a system memory coupled to said processing circuitry; and

the device defined in claim 11 coupled to the processing circuitry and the system memory.

23. A printed circuit board on which is mounted the device defined in claim 11.

24. The printed circuit board defined in claim 23, further comprising:

a board memory mounted on the printed circuit board and coupled to the device.

25. The printed circuit board defined in claim 23, further comprising:

processing circuitry mounted on the printed circuit board and coupled to the device.

26. A programmable logic integrated circuit device including a plurality of programmable logic regions, the device comprising:

a storage circuit;

at least one region configured as a data conditioning and analysis circuit;

at least another region configured as a computation circuit having an input, an output, and a critical path, wherein the computation circuit is

configured to propagate signals received on the input to the output via the critical path without propagating the signals through the data conditioning and analysis circuit, and wherein the computation circuit is programmably selectively configurable to perform at least one arithmetic operation on input data supplied from the storage circuit to produce output data; and

a datapath configured to convey the output data from the computation circuit to the storage circuit, wherein the output data on the datapath are propagated through the data conditioning and analysis circuit.

27. The device defined in claim 26, wherein the data conditioning and analysis circuit comprises at least one word conditioning subcircuit and at least one analysis subcircuit.

28. The device defined in claim 27, wherein the data conditioning and analysis circuit is configured to be programmably selectively operable in a plurality of alternative modes, wherein in a first mode, the word conditioning subcircuit is in operation, and wherein in a second mode, the analysis subcircuit is in operation.

29. The device defined in claim 27, wherein the word conditioning subcircuit is configured to be operated in series with the analysis subcircuit.

30. The device defined in claim 26, wherein the data conditioning and analysis circuit comprises:

rounding logic;

saturation logic; and

block floating point analysis logic.

31. A digital processing system, comprising:

processing circuitry;

a system memory coupled to said processing circuitry; and

the device defined in claim 26 coupled to the processing circuitry and the system memory.

32. A printed circuit board on which is mounted the device defined in claim 26.

33. The printed circuit board defined in claim 32, further comprising:

a board memory mounted on the printed circuit board and coupled to the device.

34. The printed circuit board defined in claim 32, further comprising:

processing circuitry mounted on the printed circuit board and coupled to the device.